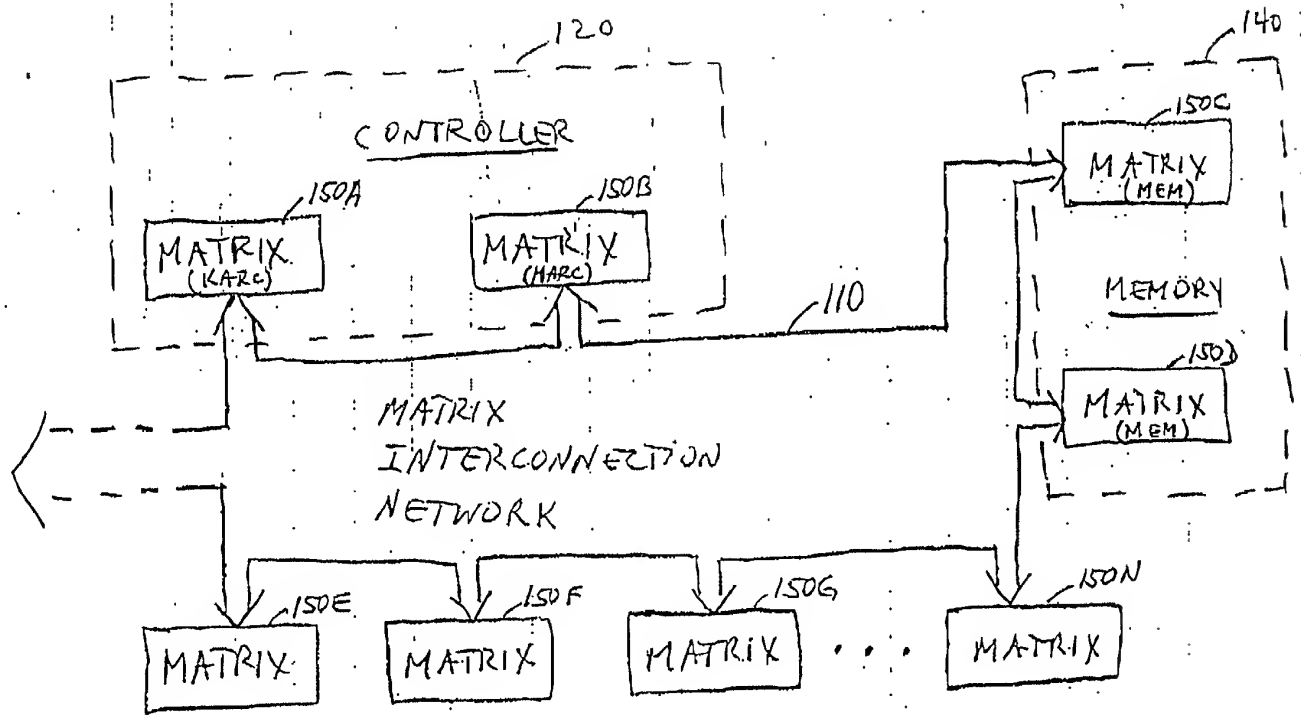


100

ADAPTIVE COMPUTING ENGINE (ACE)

FIG. 1

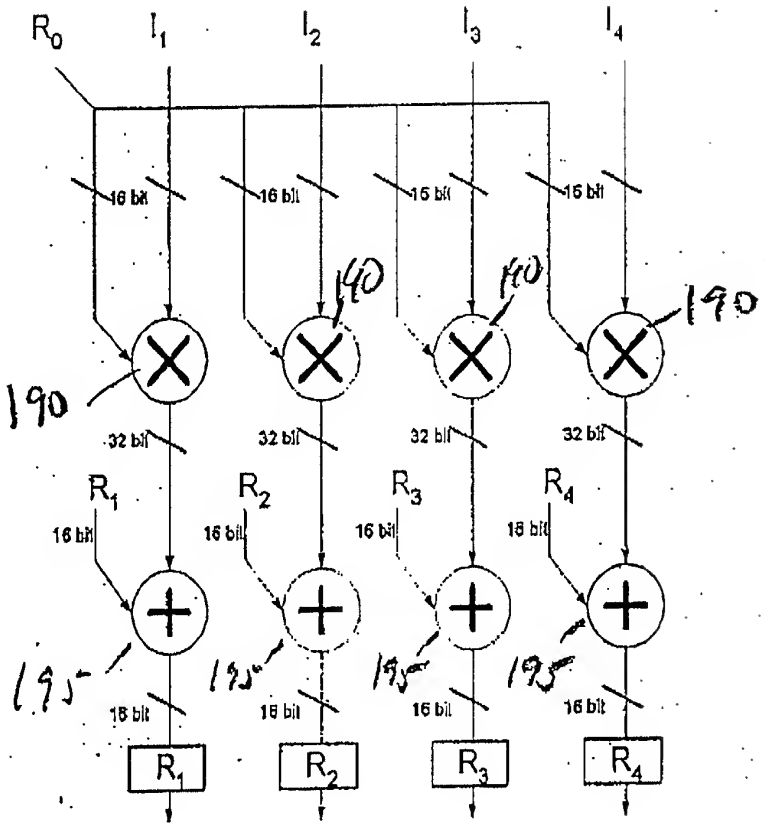


FIG. 2

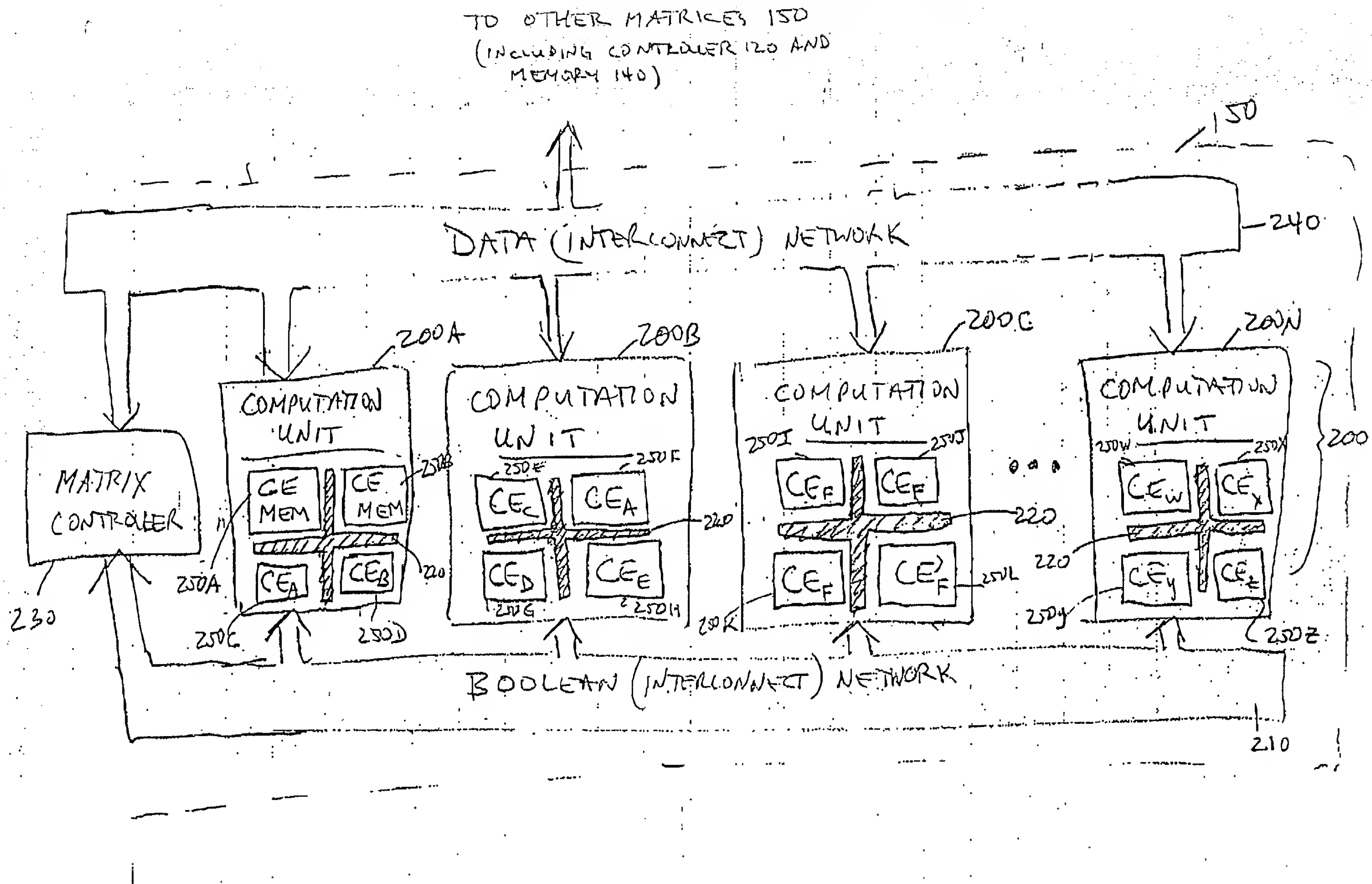

TO OTHER MATRICES 150
(INCLUDING CONTROLLER 120 AND MEMORY 140)
150
240
DATA (INTERCONNECT) NETWORK
200A
200B
200C
200N
200
COMPUTATION UNIT
CE MEM
CE MEM
CE A
CE B
CE C
CE A
CE D
CE E
CE F
CE F
CE F
CE F
CE W
CE X
CE Y
CE Z
250A
250B
250C
250D
250E
250F
250G
250H
250I
250J
250K
250L
250W
250X
250Y
250Z
220
MATRIX CONTROLLER
230
BOOLEAN (INTERCONNECT) NETWORK
210

FIG. 3

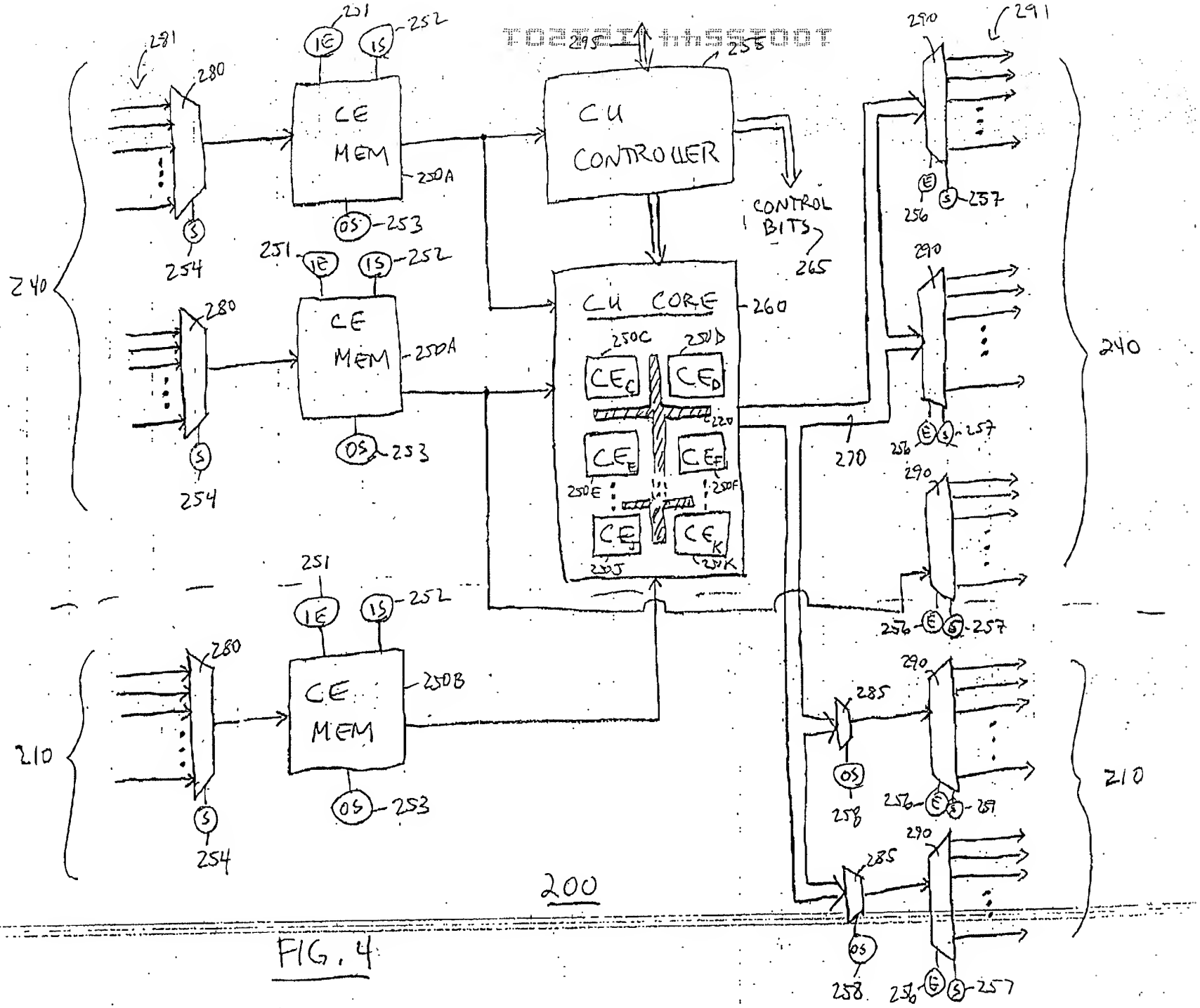

CE MEM
CU CONTROLLER
CU CORE
CONTROL BITS
265
270
240
210
200
280
290
291
250A
250B
250C
250D
250E
250F
250J
250K
251
252
253
254
255
256
257
258
285
220

FIG. 4

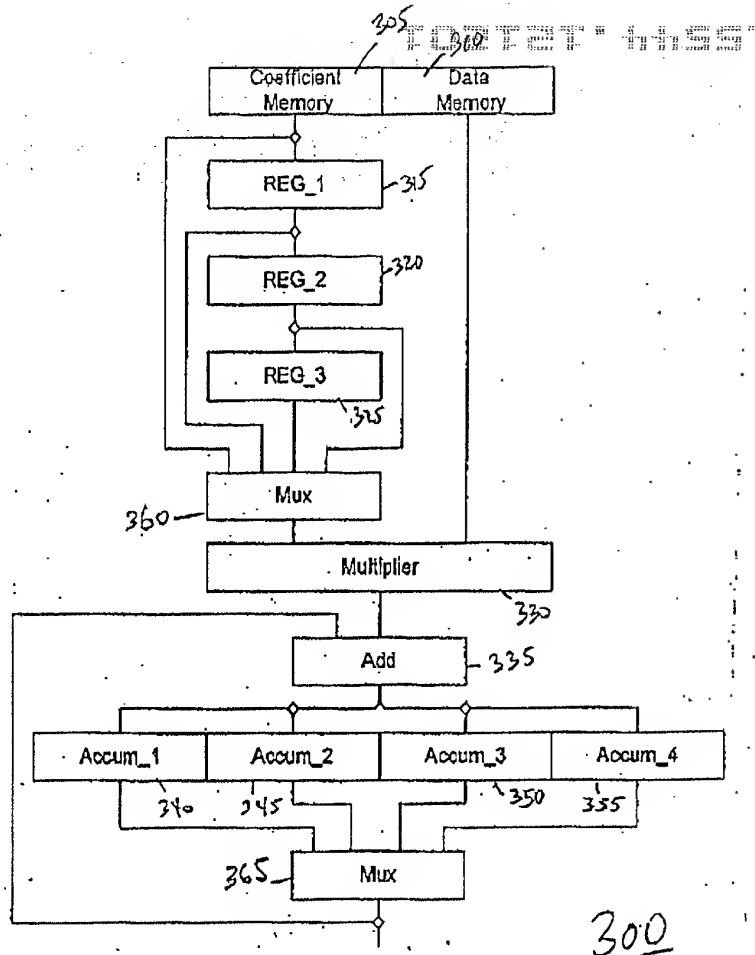

Coefficient Memory
Data Memory
REG_1
REG_2
REG_3
Mux
Multiplier
Add
Accum_1
Accum_2
Accum_3
Accum_4
Mux
300

FIG. 5A

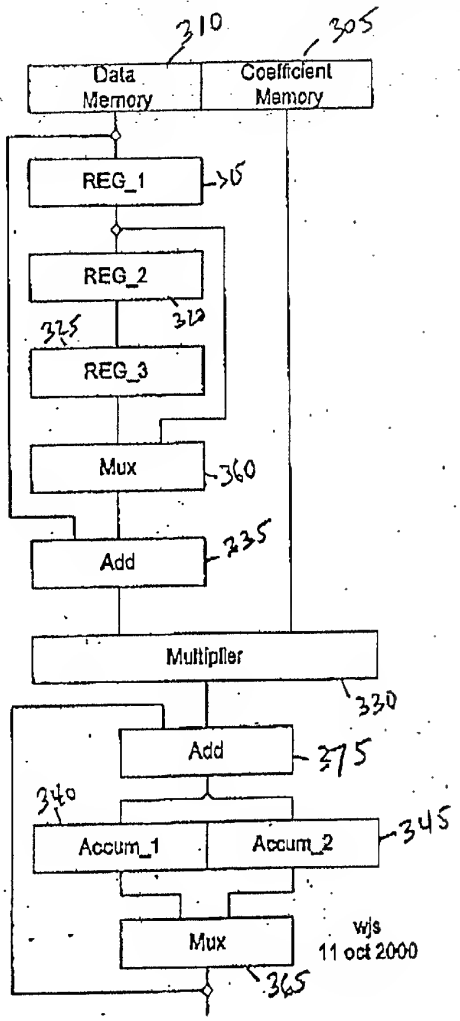
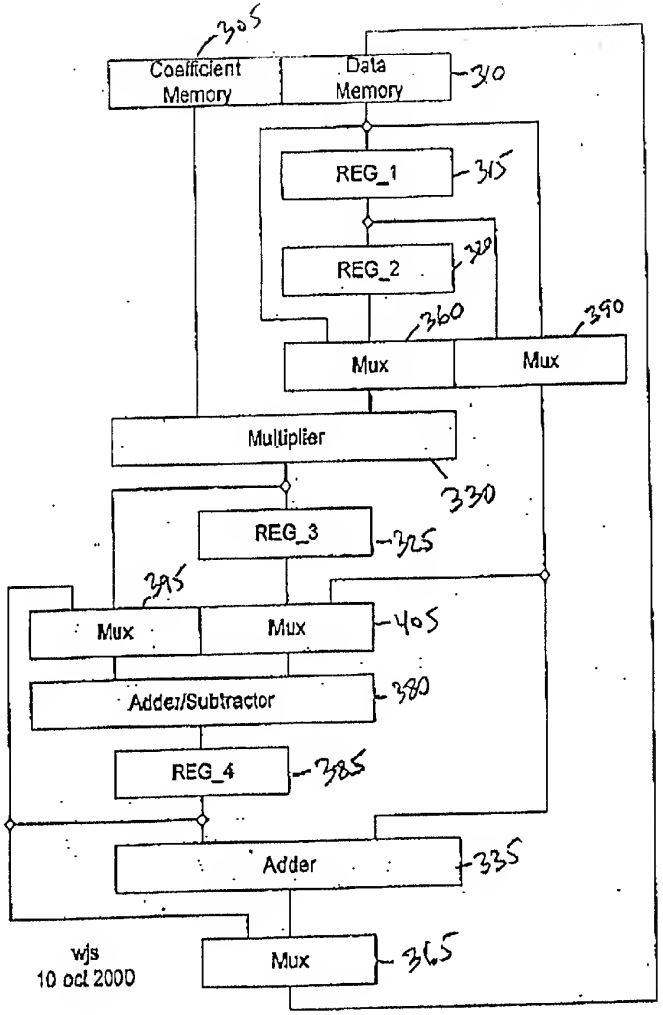


FIG. 5B


305
Coefficient Memory
Data Memory
310
REG_1
315
REG_2
320
360
390
Mux
Mux
Multiplier
330
REG_3
325
395
Mux
Mux
405
Adder/Subtractor
380
REG_4
385
Adder
335
Mux
365
wjs
10 oct 2000

400

FIG. 5C

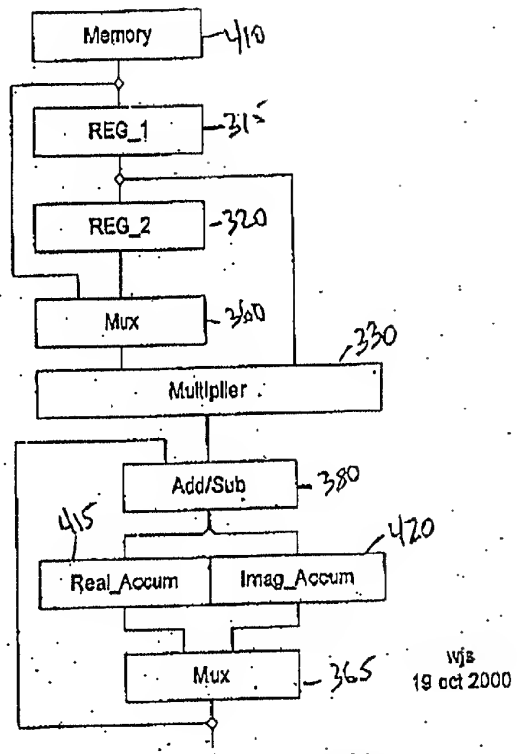

Memory
410
REG_1
315
REG_2
320
Mux
360
330
Multiplier
Add/Sub
380
415
420
Real_Accum
Imag_Accum
Mux
365
wjs
19 oct 2000
440

FIG. 5D

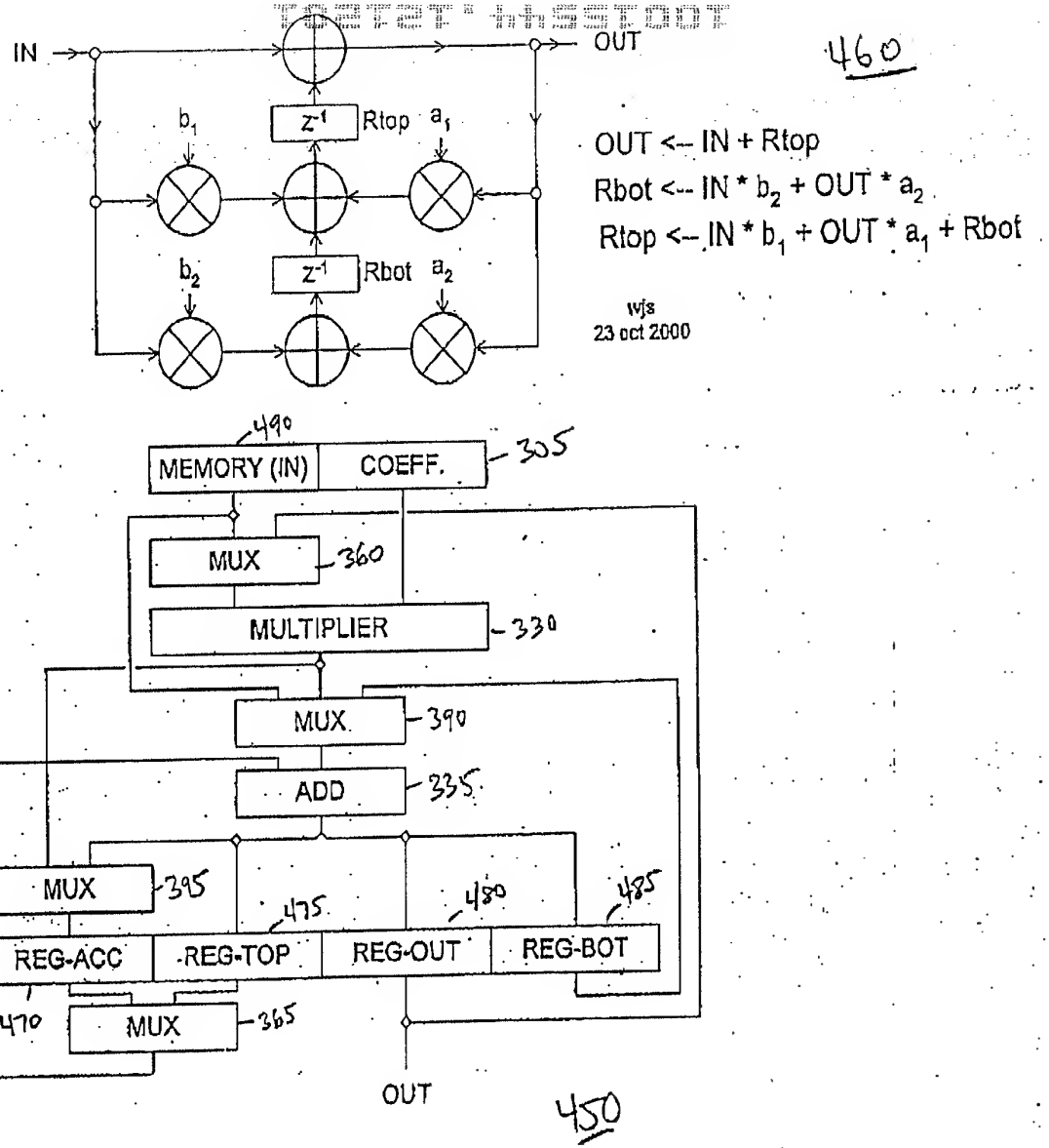

IN
OUT
460
b_1
z^{-1}
Rtop
a_1
b_2
z^{-1}
Rbot
a_2
OUT <-- IN + Rtop
Rbot <-- IN * b_2 + OUT * a_2
Rtop <-- IN * b_1 + OUT * a_1 + Rbot
wjs
23 oct 2000
490
MEMORY (IN)
COEFF.
305
MUX
360
MULTIPLIER
330
MUX
390
ADD
335
MUX
395
475
480
485
REG-ACC
REG-TOP
REG-OUT
REG-BOT
470
MUX
365
OUT
450

FIG. 5E

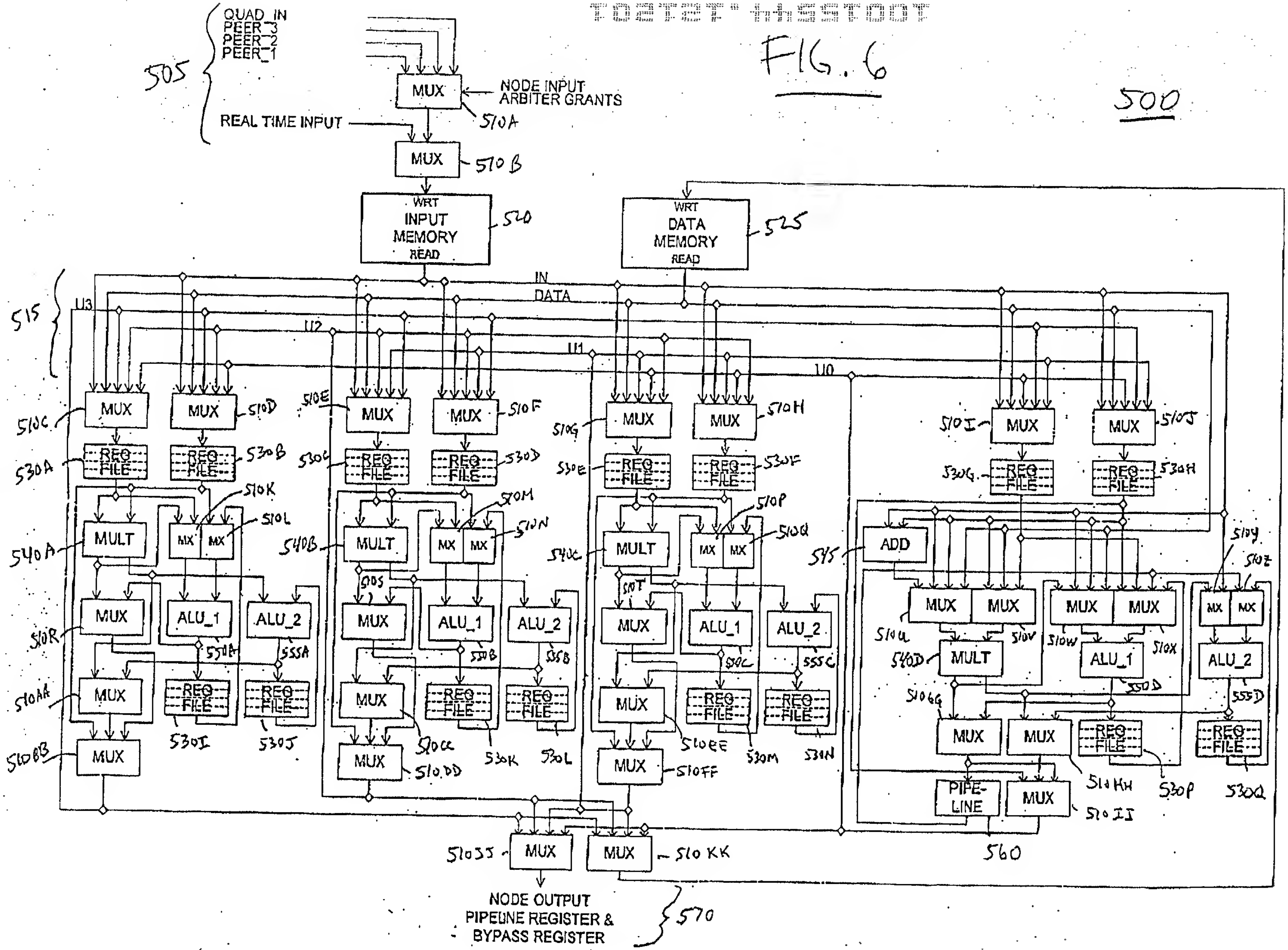

505
QUAD_IN
PEER_3
PEER_2
PEER_1
REAL TIME INPUT
MUX
NODE INPUT ARBITER GRANTS
510A
MUX
510B
WRT
INPUT MEMORY
READ
520
WRT
DATA MEMORY
READ
525
515
IN
DATA
U3
U2
U1
U0
MUX
REG FILE
MULT
MX
ALU_1
ALU_2
ADD
PIPE-LINE
510C
510D
510E
510F
510G
510H
510I
510J
530A
530B
530C
530D
530E
530F
530G
530H
510K
510L
510M
510N
510P
510Q
540A
540B
540C
540D
545
510R
510S
510T
510U
510V
510W
510X
510Y
510Z
550A
550B
550C
550D
555A
555B
555C
555D
510AA
510BB
510CC
510DD
510EE
510FF
510GG
510HH
510II
530I
530J
530K
530L
530M
530N
530P
530Q
560
510JJ
510KK
NODE OUTPUT PIPELINE REGISTER & BYPASS REGISTER
570

FIG. 6

500

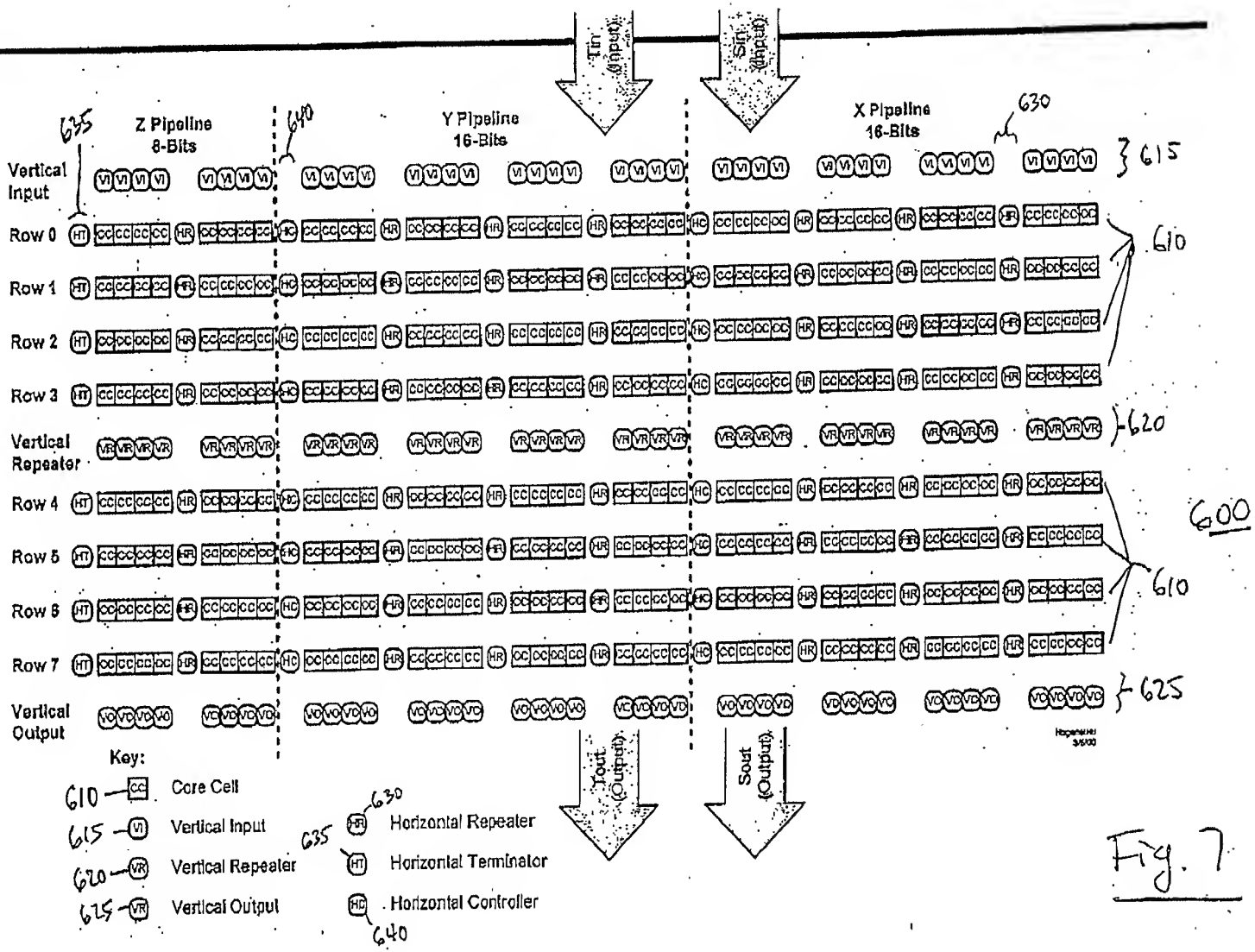


Fig. 7

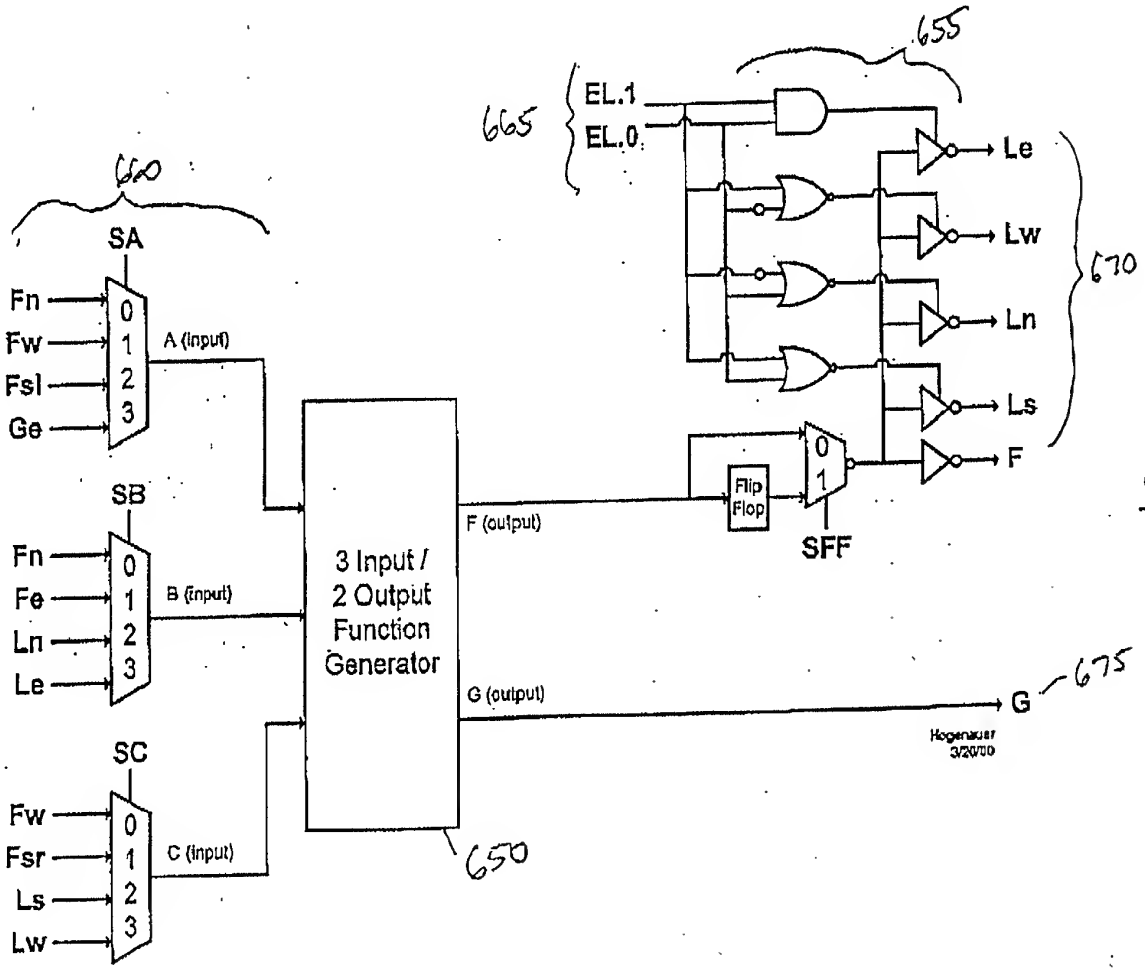


Fig. 8

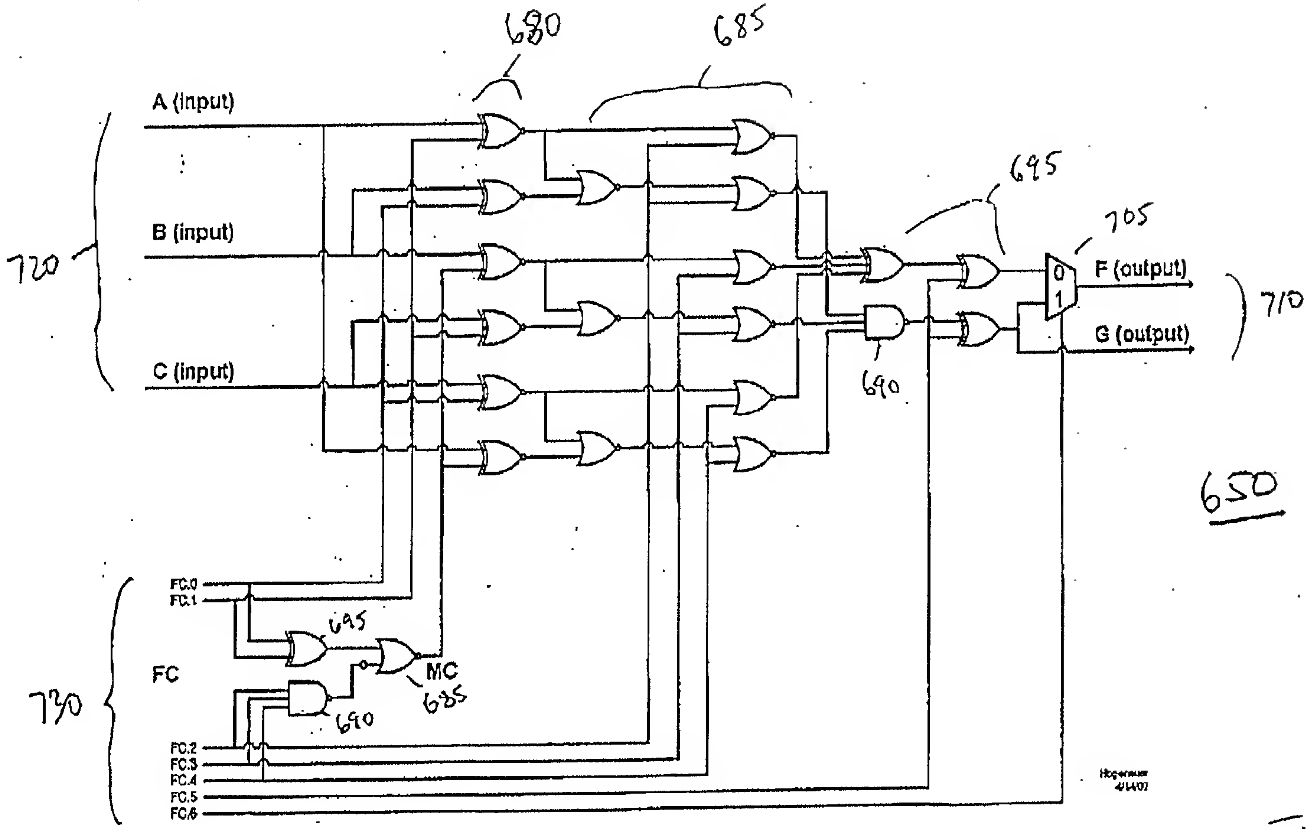
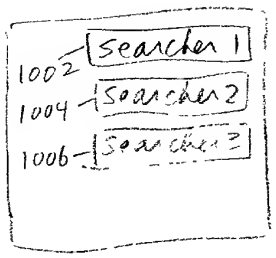
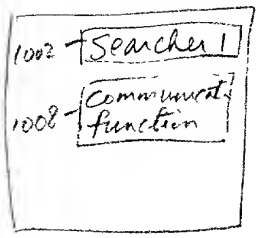

680
685
A (input)
B (input)
C (input)
720
695
705
F (output)
G (output)
710
690
650
FC.0
FC.1
695
MC
685
FC
690
730
FC.2
FC.3
FC.4
FC.5
FC.6

Fig. 9

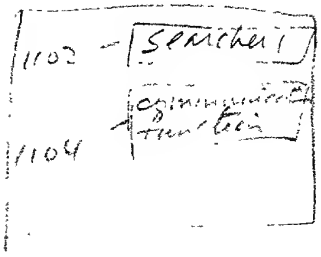


At power-up

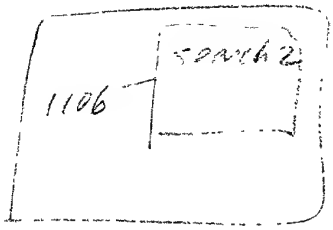


After system acquisition

FIG. 10

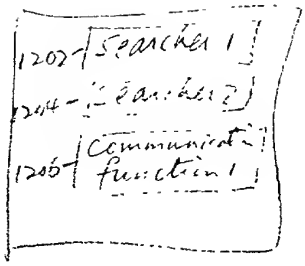


Before re-allocation

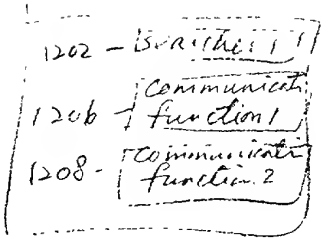


After re-allocation

FIG. 11

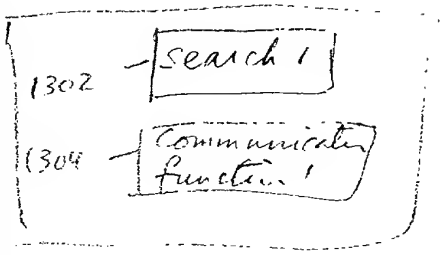


Before re-allocation

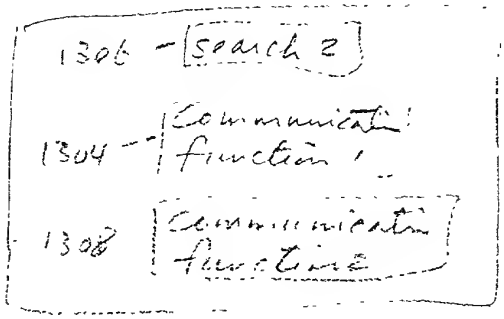


After re-allocation

FIG 12



Before re-allocation



After re-allocation

FIG. 13